



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Amold  
12/C 8/14/01  
A. W. Decker

Applicant: Hutter et al.

Art Unit: 2825

Serial No.: 09/276,780

Examiner: Luu, C.

Filing Date: 03/25/99

Docket No.: TI-27203

Title: MERGED BIPOLAR AND CMOS CIRCUIT AND METHOD

Amendment under 37 CFR 1.115

Assistant Commissioner of Patents  
Washington, DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

I hereby certify that this correspondence is being deposited with  
the U.S. Postal Service as First Class Mail in an envelope addressed  
to: Assistant Commissioner for Patents, Washington, D.C. 20231 on

8-2-01

*Marianna Smith*

Marianna Smith

Dear Sir:

The following amendment and remarks are offered in response to the  
Examiner's Office Action dated 04/11/01. They are respectfully submitted as a  
full and complete response to that Action.

Please amend the application as follows:

In the claims:

Amend claim 1 to read as follows:

1. (amended) A method for fabricating a BiCMOS integrated circuit, comprising  
the steps of:

forming in a single implantation step a base region of a bipolar transistor  
and a p-well of an n-channel MOS transistor; and

forming in a single implantation step a collector contact well of a bipolar  
transistor and an n-well of a p-channel MOS transistor, said collector contact well

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